1   PROGRAMMABLE CURRENT SOURCE

2   AND METHODS OF USE

3

4   ## Field of the Invention

5

6   This invention relates to programmable current sources for

7   use in electronic devices.

8

9   More particularly, the present invention relates to

10   programmable current sources that provide multiple current

11   source inputs to a plurality of similar circuits.

12

13

14   ## Background of the Invention

15

16   Multiple programmable current sources are generally

17   fabricated as an integrated circuit chip designed to accept

18   data and control signals as inputs and deliver constant,

19   electric currents as outputs to other electronic circuits, such

20   as light-emissive displays and other systems requiring

21   multiple, programmable current sources as inputs. Using light-

22   emissive displays as an example, such displays generally

23   consist of a matrix of rows and columns of pixels (from

24   hundreds to thousands, depending upon the size and definition

25   of the display). The rows are generally designated 0 through R

1   and the columns are designated 0 through N. It should be

2   understood that rows and columns can be interchanged throughout

3   this disclosure and no use of the terms 'rows' or 'columns' is

4   intended in any way to limit the structure or the scope of the

5   invention.

6

7   A complete screen is usually produced by cycling the rows

8   periodically from 0 to R and supplying to each column an amount

9   of current required to produce the desired luminance in each

10   pixel in the activated row. Thus, for example, when row 0 is

11   activated a current is supplied to each column 0 through N,

12   when row 1 is activated a different current (possibly) is

13   supplied to each column 0 through N, etc. Since only one row

14   of pixels is activated at a time, only the pixels in that row

15   are driven to emit light by the current applied to the columns.

16   The current applied to each column generally has a plurality of

17   steps or levels that cause the light emissive device in a pixel

18   to emit light in an equal number of steps or levels. During

19   the process of addressing each pixel in a screen, it is

20   desirable for each pixel to have the same brightness or

21   luminance for each step or level.

22

23   In many prior art constant current sources a skew or

24   mismatch is exhibited due to intrinsic device parameters in the

25   constant current source circuitry. These skews or mismatches

26   are undesirable and can occur for any type of transistor

1 topology, including but not limited to silicon based NMOS or

2 PMOS transistors. Also, while many different implementations

3 of light-emissive displays (and other systems requiring

4 multiple, programmable current sources) are possible, in most

5 instances the current must flow through a plurality of

6 components (e.g. transistors, capacitances, etc.) connected in

7 series. The intrinsic mismatch between these series components

8 and subsequent series components (e.g. between pixels in a

9 column) causes current variations between the currents flowing

10 in different columns, which produce undesired variations in

11 luminance of the pixels.

12

13 It would be highly advantageous, therefore, to remedy the

14 foregoing and other deficiencies inherent in the prior art.

15

16 Accordingly, it is an object of the present invention to

17 provide a new and improved programmable current source.

18

19 Another object of the invention is to provide a new and

20 improved programmable current source that provides matched

21 currents at multiple outputs.

22

23 And another object of the invention is to provide a new

24 and improved programmable current source and a variety of

25 calibration techniques that provides matched currents at

26 multiple outputs.

1   Still another object of the present invention is to

2   provide a new and improved programmable current source that can

3   be easily incorporated with virtually any circuitry requiring

4   multiple constant current outputs.

5

6   Yet another object of the invention is to provide a new

7   and improved programmable current source that is relatively

8   easy and inexpensive to integrate on a single chip.

Summary of the Invention

Briefly, to achieve the desired objects of the instant invention in accordance with a preferred embodiment thereof, provided is a programmable multiple current source including a plurality of current source circuits each including current level data storage circuitry. A current level data input terminal and a control input terminal are connected to each of the plurality of current source circuits to supply current level data to the storage circuitry in each of the plurality of current source circuits. Peak detector and storage circuitry is coupled to each of the output terminals of the plurality of current source circuits and includes a peak signal output terminal. Each associated current source circuit of the plurality of current source circuits includes a master digital-to-analog converter coupled to the current level data storage circuitry of the associated current source circuit, a driver circuit having an input coupled to the master digital-to-analog converter and an output coupled to the output terminal of the associated current source circuit, comparator and storage circuitry having a first input coupled to the peak signal output terminal of the peak detector and storage circuitry, a second input coupled to the output of the driver circuit, and an output, and current level adjustment circuitry coupled to the output of the comparator and storage circuitry and the input of the driver circuit.

1 The desired objects of the instant invention are further

2 realized in accordance with a preferred method of calibrating a

3 programmable multiple current source. The method includes a

4 step of providing a plurality of current source circuits each

5 including current level data storage circuitry, each of the

6 plurality of current source circuits including an output

7 terminal, and each of the plurality of current source circuits

8 being constructed to operate at a plurality of current levels

9 from a maximum current level to a minimum current level. The

10 method also includes a step of supplying current level data

11 representative of one current level in the plurality of current

12 levels to the current level data storage circuitry in each of

13 the plurality of current source circuits. Further steps in the

14 method include receiving a plurality of output signals, one

15 each representative of output current at each output terminal

16 of the plurality of current source circuits and sensing a peak

17 output signal in the plurality of received output signals,

18 comparing the output signal representative of output current at

19 each output terminal of the plurality of current source

20 circuits to the sensed peak output signal to determine a

21 difference and generating a plurality of adjustment signals,

22 one each representative of the difference for each of the

23 plurality of current source circuits, storing the plurality of

24 adjustment signals, one each for each of the plurality of

25 current source circuits, and using the stored plurality of

26 adjustment signals, one each for each of the plurality of

1   current source circuits, to adjust the output current at each

2   output terminal of the plurality of current source circuits so

3   that all of the plurality of current source circuits provide

4   substantially matching output currents.

5

6   In one specific use of the subject apparatus and method a

7   light-emissive display is provided with a plurality of pixels

8   arranged in an array of rows and columns and the plurality of

9   current source circuits are connected, one each, to each column

10   of the display.

<u>Brief Description of the Drawings</u>

2

3   The foregoing and further and more specific objects and

4   advantages of the instant invention will become readily

5   apparent to those skilled in the art from the following

6   detailed description of a preferred embodiment thereof taken in

7   conjunction with the drawings, in which:

8

9   FIG. 1 illustrates a programmable current source chip

10   coupled to a system using multiple, programmable current source

11   inputs;

12

13   FIGS. 2 and 3 illustrate typical constant current source

14   circuits that exhibit a current skew problem;

15

16   FIG. 4 illustrates a typical example of the problem of

17   providing matched currents at multiple outputs;

18

19   FIG. 5 is a general example of the use of a programmable

20   current source that provides multiple matched currents in

21   accordance with the present invention;

22

23   FIG. 6 is a schematic of a programmable current source

24   chip in accordance with the present invention; and

1   FIG. 7 is a schematic of a specific embodiment of a

2   programmable current source chip in accordance with the present

3   invention.

Detailed Description of the Preferred Embodiment

2

3   Turning now to the drawings in which like reference

4   characters indicate corresponding elements throughout the

5   several views, attention is first directed to FIG. 1 which

6   illustrates, generally, an electronic system 10 that includes a

7   programmable current source integrated circuit chip 12 and an

8   electronic circuit 14 connected to receive a plurality of

9   currents N on a similar plurality of output leads 0 through N.

10   Circuit 14 can be any circuit or application, such as a light

11   emissive display, that requires multiple programmable current

12   source inputs.   Current source 12 accepts data and control

13   signals on buses 16 and 18, respectively, and delivers

14   programmed constant electric currents on output leads 0 through

15   N to circuit 14.   The problem that arises is that prior art

16   constant current sources exhibit skew or mismatch due to

17   intrinsic device parameters.

18

19   Referring additionally to FIG. 2, an example of a typical

20   prior art constant current source 20 is illustrated.   In source

21   20 a pair of PMOS transistors P1 and P2 are formed on a common

22   chip and connected directly in parallel to conduct equal or

23   matching currents.   However, despite the transistors being the

24   same size, because of intrinsic parametric differences

25   introduced during fabrication the currents flowing through

26   transistors P1 and P2 will not be equal. Referring additionally

1   to FIG. 3, an example of a typical prior art constant current

2   source 22 is illustrated. In source 22 a pair of NMOS

3   transistors N1 and N2 are formed on a common chip and the gates

4   are connected directly in parallel to a common source current

5   so that transistors N1 and N2 are expected to conduct equal or

6   matching currents. However, despite the transistors in both

7   cases being the same size (i.e. P1=P2, N1=N2), because of

8   intrinsic parametric differences introduced during fabrication

9   the currents flowing through transistors P1 and P2 or N1 and N2

10   will not be equal. The differences may be very small but in

11   an industry which must capitalize on the use of very small

12   currents, the differences between currents flowing in

13   transistors P1/P2 and N1/N2 can be a substantial problem.

14

15   Turning now to FIG. 4, a schematic diagram of an example

16   of a typical light emissive display 25 connected to a

17   programmable multiple current source 26 is illustrated. Light

18   emissive display 25 is represented by only three pixels in a

19   single row to simplify the example. It will be understood

20   however, that display 25 will generally include hundreds, or

21   even thousands, of similar pixels in each row and hundreds, or

22   even thousands, of rows. As can be seen in FIG. 4, each pixel

23   includes a plurality of thin film transistors (TFTs) and an

24   LED, or light emissive device. Current flowing from current

25   source 26 flows through any pixels activated by a voltage on

26   the lead V_{ROW}. Also, current flowing through any pixel must

11

1 flow through several components connected in series (e.g. $TFT1_0$

2 and $TFT2_0$) and the LED to a current return terminal. The

3 intrinsic mismatch between the series connected devices in each

4 pixel (e.g. the difference between the series circuit $TFT1_0$,

5 $TFT2_0$ and the LED and the series circuit $TFT1_N$, $TFT2_N$ and the

6 LED) causes variations in the currents (in this specific

7 example $I_{PIXEL(0)}$ and $I_{PIXEL(N)}$). These current variations cause

8 undesired variations in luminance of the pixels.

9

10 Turning now to FIG. 5, a simplified block diagram of a

11 programmable multiple current source 30 in accordance with the

12 present invention is illustrated in connection with a typical

13 light emissive display for purposes of illustration. In this

14 example, programmable multiple current source 30 provides

15 multiple (N) matched currents to a light emissive display 32

16 consisting of R rows and N columns of pixels. A controller

17 circuit or chip 34 sends data codes and data control signals to

18 current source 30 causing current source 30 to deliver N

19 matching current outputs to the N columns of display 32. A row

20 driver chip 36 delivers excitation voltage to each of the R

21 rows of display 32 in a regular cycle (i.e. row 0, row 1, etc.

22 through row R and then back to row 0) in response to timing or

23 control signals supplied by controller chip 34.

24

25 Referring additionally to FIG. 6, a more detailed

26 schematic of programmable multiple current source 30 is

12

1   illustrated. Multiple current source 30 includes a plurality

2   of current source circuits $40_{(0)}$ through $40_{(N)}$ each including

3   current level data storage circuitry. In this embodiment the

4   current level data storage circuitry in each associated current

5   source circuits $40_{(0)}$ through $40_{(N)}$ includes a register 42 and a

6   latching circuit 44. A current level data input terminal and

7   bus 46 and a control input terminal and bus 48 are connected to

8   each of the plurality of current source circuits $40_{(0)}$ through

9    $40_{(N)}$ to supply current level data to the storage. In this

10   example, current level data input terminal and bus 46 and

11   control input terminal and bus 48 are connected to controller

12   chip 34 (see FIG. 5). As will be understood by those skilled

13   in the art, bus 46 carries digital signals (current level data)

14   representative of a specific luminance (or driving current)

15   level for each pixel and bus 48 carries control signals that

16   direct the correct luminance signal to be stored in each

17   register 42 and latch 44 of the current source circuits $40_{(0)}$

18   through $40_{(N)}$.

19

20   For example, if light emissive display 32 is constructed

21   to operate with sixty four levels of luminance in each pixel,

22   bus 46 might have as few as six leads (it could include more

23   leads for other functions) to carry the digital code

24   representative of a specific one of the sixty four possible

25   levels. The code for each pixel of the N pixels would appear

26   in parallel on bus 46 and be clocked into the appropriate

register 42 by a timing signal on bus 48. In this example, a first six bit current level signal is clocked into register 42 in current source circuit $40_{(0)}$, a second six bit current level signal is clocked into register 42 in current source circuit $40_{(1)}$, and so on through register 42 in current source circuit $40_{(N)}$. Specific connections of bus 48 are not illustrated for simplicity and an easier understanding of the inventive portion of the system.

Each current source circuit $40_{(0)}$ through $40_{(N)}$ includes a master digital-to-analog converter 50 coupled to the current level data storage circuitry of the associated current source circuit. In each of the current source circuits, digital-to-analog converter 50 receives the six bit digital signal (in this example) from latch 44 and converts it to the appropriate analog signal, which is then applied to a column driver circuit 52. The output of each of the N driver circuits 52 is applied to an output terminal $I_{(0)}$ through $I_{(N)}$ of the associated current source circuit $40_{(0)}$ through $40_{(N)}$. The outputs of all of the N driver circuits 52 are also applied through N switches 54 to the input of peak detector and storage circuitry, which in this embodiment includes a peak detector 56 and a level shift circuit 58. In this embodiment switches 54 are illustrated as single-pole single-throw switches but it will be understood that this is simply a schematic representation and some form of semiconductor may be used so as to be integrated into the chip.

Each current source circuit $40_{(0)}$ through $40_{(N)}$ also includes comparator and storage circuitry, which in this embodiment includes a comparator 60 and some convenient form of memory 62. Each comparator 60 includes an input connected to an output of level shift circuit 58 for receiving a signal representative of a peak signal. Each comparator 60 also includes an input connected to driver circuit 52 of the associated current source circuit for receiving an output signal representative of the drive signal at the output $I_{(0)}$ through $I_{(N)}$ of the associated current source circuit. Comparator 60 compares the two input signals and supplies a signal representative of the difference to memory 62. An oscillator 64 and counter 66 may optionally supply a signal to an input of memory 62 for incrementing addresses in memory 62 or for converting the difference signal in comparator 60 to a digital signal for convenient storage in memory 62, as will be described in more detail presently.

An output signal from memory 62 is supplied to an adjustment circuit 68, which supplies an analog compensation or adjustment signal, in conjunction with the analog signal from digital-to-analog converter 50, to the input of driver circuit 52. The analog adjustment signal is specifically generated to bring the drive signal at the output of driver circuit 52, in each of the current source circuits $40_{(0)}$ through $40_{(N)}$ into a substantially matching level or state when the same current

15

level data input signal is applied. Generally, the adjustment

signal will change or adjust the input signal to driver circuit

52 a small amount or some convenient amount (e.g. a fraction of

a level or one complete level). In the preferred method (which

will be described presently), the adjusted output signal of

driver circuit 52 is again compared to the peak signal in

comparator 60 and a second adjustment is generated, if

necessary. The adjustment cycle is continued until the output

of driver circuit 52 matches the peak signal in comparator 60,

at which time the final adjustment signal is stored in

adjustment circuit 68 and comparator 60 latches memory 62 to

stop or deactivate the process. In some specific adjustment

methods, adjustment circuit 68 may use the digital current

level data signal stored in latch 44, and, accordingly, a

connection for that purpose is illustrated.

A variety of methods for adjusting the driver current at

the current outputs $I_{(0)}$ through $I_{(N)}$ of programmable multiple

current source 30 to achieve substantially matched currents are

possible.   For convenience in understanding the present

invention and its operation, three potential methods of

adjustment are described below. Further, each of the methods

is performed during a calibration period that may be performed

at any convenient time, e.g. when the display is first turned

on, periodically (every half-hour, hour, etc.), or whenever a

change in the display is sensed.   It will of course be

understood by those skilled in the art that modifications of the described methods and other completely different methods may be devised.

In a first method of adjusting or matching the driver current at the current outputs $I_{(0)}$ through $I_{(N)}$, a calibration period includes a calibration cycle performed for each row, row 0 through row R. In the first calibration cycle, a maximum illumination level signal is applied by way of bus 46 to register 42 in each of the current source circuits $40_{(0)}$ through $40_{(N)}$ with row 0 of pixels activated. All N switches 54 are closed sequentially so that all N outputs are applied sequentially to peak detector 56 and the peak output is sensed. The peak output is stored and simultaneously applied to each comparator 60 in each current source circuit $40_{(0)}$ through $40_{(N)}$. The comparison and adjustment cycle described above is performed in each current source circuit $40_{(0)}$ through $40_{(N)}$ until the outputs of all current source circuit $40_{(0)}$ through $40_{(N)}$ match at the maximum level with row 0 of pixels activated. The final adjustment signal generated by adjust circuit 68 is stored for use each time row 0 is activated.

A second calibration cycle is then performed with row 1 activated, a third calibration cycle is performed for row 2, and so on through all R rows. In each cycle the final adjustment signal is stored and used each time that row is

17

1   activated. Thus, R final adjustment signals are stored in each

2   of the N adjustment circuits 68 and applied during actual use

3   of display 32. In this method, it is assumed that the amount

4   of adjustment required at each level of illumination for each

5   pixel will be approximately the same. While a maximum level is

6   used throughout the calibration period, it will be understood

7   that any other level (e.g. one of the mid levels) could be used

8   to develop the amount of adjustment signal required for

9   matching all of the outputs.

10

11   In another method of adjusting or matching the driver

12   current at the current outputs $I_{(0)}$ through $I_{(N)}$, a calibration

13   period includes a calibration cycle performed for each row, row

14   0 through row R. In this method, during a calibration cycle, a

15   pre-selected list of specific level codes are cycled into each

16   register 42 in each of the current source circuits $40_{(0)}$ through

17   $40_{(N)}$ with row 0 of pixels activated. The specific level codes

18   could be, for example, 10000, 010000, 001000, 000100, 000010,

19   and 000001, assuming sixty four levels of luminance or drive

20   current. In this example, adjustment circuit 68 will usually

21   include a 6-bit priority encoder. An adjustment signal is

22   generated and stored in each of the N adjustment circuits 68,

23   as described above, for each of the six specific level codes.

24   A second calibration cycle is then performed with row 1

25   activated and so on through all R rows.

18

1   Once the calibration period is completed and display 32 is

2   in normal use, as each row in a screen is activated the level

3   input data cycled into each register 42, for the pixel in the

4   activated row, is provided to adjustment circuit 68.

5   Adjustment circuit 68 determines the most significant digit in

6   the level input data and supplies the adjustment signal that

7   conforms to that digit. For example, when the level input data

8   is 000100 adjustment circuit 68 supplies the adjustment signal

9   developed for specific level code 000100, when the level input

10   data is 000101 adjustment circuit 68 supplies the adjustment

11   signal developed for specific level codes 000100 and 000001,

12   when the level input data is 000111 adjustment circuit 68

13   supplies the adjustment signal developed for specific level

14   codes 000100, 000010, and 000001, etc.

15

16   In another method, every level is adjusted in every pixel.

17   That is, in a first adjustment cycle of an adjustment period,

18   an adjustment signal is developed and stored (as described

19   above) for each of the sixty three levels (skipping of course

20   the zero or off level) of current or luminance of the current

21   source circuits $40_{(0)}$ through $40_{(N)}$ with row 0 of pixels

22   activated. In a second adjustment cycle of the adjustment

23   period, an adjustment signal is developed and stored (as

24   described above) for each of the sixty three levels (skipping

25   of course the zero or off level) of current or luminance of the

26   current source circuits $40_{(0)}$ through $40_{(N)}$ with row 1 of pixels

19

1   activated.   In this fashion an adjustment signal for each of

2   the sixty three levels is developed and stored for each pixel

3   in each row.   Because of the inordinately large number of

4   adjustment signals (63 times R for each column in this example)

5   that must be stored in this method, it is not a preferred

6   method at this time.

7

8   Referring to FIG. 7, the preferred method of adjusting or

9   matching the driver current at the current outputs $I_{(0)}$ through

10   $I_{(N)}$, is illustrated.   In FIG. 7, components that are similar to

11   components in FIG. 6 are designated with similar numbers having

12   a prime added to indicate the different embodiment.   Also,

13   components described in conjunction with FIG. 6 will not be

14   further described unless additional or different functions are

15   performed.   In this embodiment, adjustment circuit 68 is

16   replaced with a process block 68' and an adjustment digital-to-

17   analog converter 69', the output of which is added to the

18   output of digital-to-analog converter 50' by a summing circuit

19   67'.   It should be noted that in this embodiment a voltage is

20   sensed at the output of driver 52' (even though schematically

21   it is connected to the current output) and supplied to

22   comparator 60'.   Also, the output signal from level shift

23   circuit 58' is a voltage, since voltages are generally easier

24   and more accurate to sense and compare.   The topology of

25   process block 68' can be defined as the algorithm

1 .   ADJUST FACTOR = $(((A)/2^{(K)})*(B))$

2   Where: A = the J-bit vector output from memory 62',

3   B = the K-bit vector output from latch 44', and

4   K = the number of bits used for the level code.

5

6   In this method, the adjustment is solely made for the

7   full-scale output current level, 111111, in this example. The

8   adjustment signal is determined for each row R in the display

9   and stored in memory 62'. The adjustment signal applied to the

10 adjustment I-DAC 69' is scaled by processor 68', based on the

11 aforementioned adjust factor equation and the value appearing

12 at the output of master latch 44'.

13

14   Thus, a new and improved programmable current source that

15 provides matched currents at multiple outputs is described. A

16 variety of calibration techniques can be used with the new and

17 improved programmable current source to provide matched or

18 substantially matched currents at multiple outputs. Here it

19 will be understood that not all of the methods described

20 provide adjustments for exact matching of all pixels for all

21 levels of luminance but all of the methods described provide

22 multiple outputs that are more closely matched than any known

23 prior art circuits, structures, or devices. The multiple

24 programmable current source can relatively easily be

25 incorporated with virtually any circuitry requiring multiple

1   constant current outputs and is relatively easy and inexpensive

2   to integrate on a single chip.

3

4   Various changes and modifications to the embodiment herein

5   chosen for purposes of illustration will readily occur to those

6   skilled in the art. For example, while the described

7   calibration methods use specific levels other or additional

8   levels could be used, fewer rows of pixels could be involved in

9   the calibration methods, depending on the specific application

10   or applications for which is intended to be employed. To the

11   extent that such modifications and variations do not depart

12   from the spirit of the invention, they are intended to be

13   included within the scope thereof.

14

15   Various changes and modifications to the embodiments

16   herein chosen for purposes of illustration will readily occur

17   to those skilled in the art. To the extent that such

18   modifications and variations do not depart from the spirit of

19   the invention, they are intended to be included within the

20   scope thereof which is assessed only by a fair interpretation

21   of the following claims.

22

23   Having fully described the invention in such clear and

24   concise terms as to enable those skilled in the art to

25   understand and practice the same, the invention claimed is: